Attached hereto is a marked-up version of the changes made by current amendment. The attached pages are captioned **"Version with Markings to Show Changes Made"**.

Kindly consider the following remarks:

REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1 to 14 are pending in the application. Claims 1 to 14 have been rejected. Claims 1 through 6 have been amended.

Claims 1 through 14 have been voluntarily amended for clarification only. These amendments do not narrow the scope of the claim, nor have they been made for reasons of patentability.

Applicants respectfully assert that the amendments to the claims add no new matter.

The Telephone Interview

Applicants wish to thank the Examiner, Hoai V. Hofor having a telephone conversation with Applicants' Representative, Vladimir Sherman, Reg. No. 43,116. During the conversation, an apparent error in paragraph 12 of the Office Action was discussed. The

Examiner rejected claims 1 to 38 and 41 to 48 in error, since only claims 1 to 14 are pending in the current application. Applicants' Representative and the Examiner agreed to interpret the rejections in paragraph 12 of the Office Action as rejections of claims 1 to 14.

CLAIM REJECTIONS

35 U.S.C. § 112 Rejections

In the Office Action, the Examiner rejected claims 1 through 14 under 35 U.S.C. § 112, second paragraph, for allegedly "omitting essential steps". More specifically, claim 1 has been rejected for omitting "how do programming pulses apply to which terminal of three terminals, the gate, source, and drain, of a memory cell." Claims 2 through 14 have been rejected for incorporating the defect of claim 1. Claim 1 has been amended to recite: "A method for programming a memory array, the method using programming pulses applied to either the drain or gate of one or more memory cells within said memory array...". It is respectfully asserted that the foregoing amendment merely addresses matters of form and does not change the literal scope of the claim in any way or result in any prosecution history estoppel. Applicants respectfully assert that these amendments over the above state 35 USC 112 rejections of claims 1 through 14, and request that the rejections be withdrawn.

In the Office Action, the Examiner rejected claims 2, 3, 5, and 6 under 35 U.S.C. § 112, second paragraph, as allegedly "being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention". More specifically:

In claim 2 - The Examiner alleged that the term "fast bit" is unclear and that there is no support for the terms "the fastest bit" and "the general vicinity." Claim 2 has been amended to overcome these rejections.

In claim 3 – The Examiner alleged that the it was unclear how a "fast bit" relates to "all of the bits of said memory array. Claims 2 and 3 have been amended to recite "a fast bit of said memory array having a relatively faster programming characteristic than other bits in said array." This amendment should make it clear to anyone of ordinary skill in the art what is the relation between the "fast bit" and the rest of the bits in the array.

In claim 3 – The Examiner alleged that the phrase "programming generally all of the bits of said memory array" is confusing. Applicants are confused by the Examiner's position. One of ordinary skill in the art should know what it means to program a memory cell. Furthermore, one with an average command of the English language should know what "generally all" means. Therefore, Applicant does not see where there is room for misunderstanding? Therefore, with all due respect, Applicants respectfully request that the Examiner withdraw the above stated rejection of claim 3.

In claim 3 – The Examine alleged that there was insufficient antecedent basis for the term "a programming pulse level." Claim 3 has been amended to recite a "programming pulse voltage level." Applicants believe this amendment renders the Examiner's rejection moot.

In claims 5 and 6 – The Examiner alleged that the phrases starting with "wherein said generally all of the bits is all of the bits of the array..." are unclear. Claims 5 and 6 have been amended in view of the rejection, and Applicants believe the Examiner's above stated rejections have been addressed such that these phrases in claims 5 and 6 are now clear.

35 U.S.C. § 102 Rejections

In the Office Action, the Examiner rejected claims 1 to 14 under 35 U.S.C. § 102(a), as being anticipated by U.S. Pat. No. 6,292,394 to Cohen et al. The Examiner also rejected claims 1 to 14 under 35 U.S.C. § 102(b), as being anticipated by U.S. Pat. No. 5,870,335 to Khan et al. Applicants respectfully disagree with these rejections. More specifically:

Amended Independent claim 1 now recites "A method for programming a memory array....the method comprising...adapting the duration or the amplitude of said programming pulses as a function of the current state of said memory array."

Whereas, The Cohen reference teaches:

> "A method for programming an array having a multiplicity of memory cells. The method includes, per cell to be programmed, verifying a programmed or non-programmed state of the cell and flagging those of the cells that verify as non-programmed during one of the verify steps after having previously verified as programmed. A programming pulse having a programming level is applied to the non-programmed cells which are not flagged cells. The steps of verifying, flagging and applying are then repeated

> until all of the cells verify as programmed at least once. Subsequently, a boost pulse having a boost programming level lower than the programming level is applied to the flagged cells." (Cohen reference Abstract)

And whereas, The Kahn reference teaches:

> "An integrated circuit memory system and method for precision hot carrier injection programming of single or plurality of nonvolatile memory cells is described. Each program cycle is followed by a verify cycle. Precision programming is achieved by incrementally changing a programming current pulse flowing between the source and drain in the memory cell during successive program cycles and a constant current during successive verify cycles. Current control and voltage mode sensing circuitry reduces circuit complexity, reduces programming cell current, lowers power dissipation, and enables page mode operation. Precision programming is useful for multilevel digital and analog information storage." (Kahn reference Abstract)

Neither the Cohen nor the Kahn references teach or suggest "adapting the duration or the amplitude of said programming pulses as a function of the current state of said memory array." To the contrary, the programming pulse voltage levels and durations in the two references are predefined and not adapted based on the state of the array. Applicants, therefore, respectfully request reconsideration and withdrawal of the rejections of independent claim 1. Since claims 2 through 14 depend from claim 1, Applicants believe claims 2 to 14 to be allowable by virtue of their dependence on an allowable base claim.

Double Patenting Rejections

In the Office Action, the Examiner rejected claims 1 through 14 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9 and 13- 15 of U.S. Pat. No. 6,396,741. For the same reason's stated above regarding the 102 rejections based on the Cohen and Kahn references, Applicants believe that claims 1 to 14 are patentably distinct from claims 1, 9 and 13 through 15 of the '741 patent.

Applicants note that none of the amendments to the claims herein are in response to the above discussed prior art rejections.

In view of the foregoing amendments and remarks, all pending claims are believed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 05-0649.

Respectfully submitted,

Vladimir Sherman
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Dated: December 5, 2002

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In the Claims:

1. A method for programming a memory array, the method using programming pulses applied to either the drain or gate of one or more memory cells within said memory array, the method comprising [the step of]:

adapting the duration or the amplitude of said programming pulses [to the] as a function of the current state of said memory array.

2. A method according to claim 1 wherein said step of adapting includes[the steps of]:

determining the voltage level of the programming pulse used to program [generally the fastest] a fast bit of said memory array having a relatively faster programming characteristic than other bits in said array; and

setting an initial programming pulse voltage level [of said memory array] to a level [in the general vicinity of] near said programming pulse voltage level of said [generally] fast bit.

3. A method according to claim 2 and wherein said step of determining includes [the steps of]:

programming a small set of bits of said memory array;

setting a starting programming pulse voltage level to a programming pulse voltage level not higher than [the] a programming pulse voltage level used to program a fast bit of said small set having a relatively faster programming characteristic than other bits in said small set;

programming generally all of the bits of said memory array using pulses having voltage levels beginning at said starting programming pulse voltage level; and

setting said initial programming pulse voltage level to a programming pulse level [in the general vicinity of] near a programming pulse voltage level [of a fast] used to program a bit having a relatively faster programming characteristic than [of] generally all other [of said] bits of said array.

4. A method according to claim [1] 2 wherein said [general vicinity] initial programming pulse voltage level is not higher than said programming pulse level of said fast bit.

5. A method according to claim 3 wherein said generally all of [the] bits of said array does not include [is all the bits of the array but the] bits of said small set.

6. A method according to claim 3 wherein said generally all of [the] bits of said array does include [is all of the] bits of said small array.